We Claim:

1. In a semiconductor memory module divided into banks and having an address structure in which each address is associated with a bank organized in rows and columns and defined with a row address, a column address, and a bank address, a method for comparing a memory access address with a known address of a faulty memory cell, the method which comprises:

in a first cycle, activating one row using a row address and an associated bank address;

in a second cycle, accessing the activated row using a column address and a bank address;

during the activation of the row:

a) comparing the row address of the activated row with the row address of the faulty memory cell, and passing a comparison result to a latching circuit outputting an output signal to a logic stage;

b) comparing the bank address with the bank address of the faulty memory cell passing a bank address comparison result to the logic stage;

c) comparing the column address with the column address of the faulty memory cell and passing the comparison result to the logic stage;

d) obtaining an activation pulse from a rising flank of a bank selection signal in a pulse generator and passing the activation pulse to the latching circuit if the bank address comparison result indicates a match and an enable register is set;

e) outputting a latching signal with the latching circuit if the comparison result in step a) is positive and an activation pulse has arrived from step d); and

outputting a hit signal with the logic stage, the hit signal indicating access to a faulty memory cell, if the comparison results in steps b) and c) are positive and the latching circuit is outputting the latching signal.